AMENDMENTS TO THE CLAIMS:

Please cancel claim 27 without prejudice or disclaimer.

1-4. (Canceled)

5. (Currently amended) A group III nitride compound semiconductor device comprising:

a silicon substrate on which a first environment division and a second environment division are formed; and

a plurality of first group III nitride compound semiconductor layers formed on said first environment division so as to serve as effective semiconductor layers,

wherein said first environment division comprises a surface of said silicon substrate, said plurality of first group III nitride compound semiconductor layers being formed on said surface, ~~and~~

wherein said second environment division comprises silicon oxide formed on said surface of said silicon substrate, and

wherein said plurality of first group III nitride compound semiconductor layers comprises a plurality of stacks of first group III nitride compound semiconductor layers, said stacks being separated by said silicon oxide and not connected.

6. (Previously presented) A device according to claim 5, wherein said first group III nitride compound semiconductor layers are formed on said first environment division directly on an exposed surface of said substrate.

7. (Previously presented) A device according to claim 6, wherein said plurality of first group III nitride compound semiconductor layers are not grown on said second environment division.

8. (Previously presented) A device according to claim 6, further comprising:

a second group III nitride compound semiconductor layer, which is at least one of amorphous and different in crystallinity from said first group III nitride compound semiconductor layers, grown on said second environment division.

9. (Currently amended) A semiconductor device structure having a first portion and a plurality of second portions, said structure comprising:

a silicon substrate;

a silicon oxide separating layer formed on ~~said~~ surface of said substrate and defining a plurality of openings respectively formed in said plurality of second portions; and

a plurality of stacks of group III nitride compound layers which are respectively formed on said surface in said plurality of openings,

wherein said plurality of stacks of group III nitride compound semiconductor layers are separated by said separating layer and not connected.

10. (Previously presented) The structure according to claim 9, wherein said plurality of openings comprises one of a square and a rectangle, having a side with a length in a range from 100 to 1000μm.

11. (Previously presented) The structure according to claim 9, wherein said plurality of openings comprises one of a square and a rectangle, having a side with a length in a range from 200 to 800μm.

12. (Previously presented) The structure according to claim 9, wherein said separating layer has a thickness of about 5.5 μm.

13. (Previously presented) The structure according to claim 9, wherein a distance between adjacent ones of said openings is about 50 μm.

14. (Previously presented) The structure according to claim 9, further comprising:

an undercoat layer comprising one of a metal and a metal nitride formed over said substrate in said plurality of openings.

15. (Previously presented) The structure according to claim 9, wherein each opening of said plurality of openings has a rounded shape.

16. (Previously presented) The structure according to claim 9, wherein said separating layer is formed directly on said substrate.

17. (Currently amended) A method of forming a semiconductor device structure having a first portion and a plurality of second portions, said method comprising:

forming a silicon oxide separating layer over a surface of a silicon substrate;

forming a mask over said separating layer;

etching said separating layer using said mask to create a plurality of openings in said separating layer; and

forming a plurality of group III nitride compound semiconductor layers on said surface of said silicon substrate in said plurality of openings,

wherein said plurality of group III nitride compound semiconductor layers comprises a plurality of stacks of group III nitride compound semiconductor layers, said stacks being separated by said separating layer and not connected.

18. (Previously presented) The method according to claim 17, wherein said forming said separating layer over said substrate comprises forming said separating layer directly on said substrate, and

wherein said forming said mask over said separating layer comprises forming said mask directly on said separating layer.

19. (Previously presented) The structure according to claim 9, wherein said group III nitride compound semiconductor layers are not formed on said separating layer.

20 - 22 (Canceled)

23. (Previously presented) The structure according to claim 9, wherein said plurality of openings comprises one of a square having rounded corners and a rectangle having rounded corners.

24. (Currently amended) A method of forming a group III nitride compound semiconductor device, said method comprising:

forming amorphous ~~silicon~~ portions of a silicon substrate surface in a grid-shaped pattern by implanting ions in said silicon substrate surface; and

forming a group III nitride compound semiconductor layer on said substrate surface such that a portion of said layer formed on said amorphous ~~silicon~~ portions of said substrate surface has a different crystalline structure than a portion of said layer formed on portions of said substrate surface that are other than said amorphous ~~silicon~~ portions,

wherein said portion of said group III nitride compound semiconductor layer formed on said amorphous portions of said substrate surface is not connected to a portion of said layer formed on said portions of said substrate surface that are other than said amorphous portions.

25. (Currently amended) The method according to claim 24, wherein said portions of said substrate surface that are other than said amorphous ~~silicon~~ portions comprise square-shaped portions formed between said amorphous ~~silicon~~ portions having said grid-shaped pattern.

26. (Currently amended) The method according to claim 24, wherein said portion of said group III nitride compound semiconductor layer formed on said amorphous ~~silicon~~ portions of said substrate surface comprises a columnarly grown portion.

27. (Canceled)

28. (Previously presented) The device according to claim 5, wherein said plurality of first

group III nitride compound semiconductor layers are formed only on said first environment division.

29. (Previously presented) The device according to claim 5, wherein said first environment division comprises a rounded shape.

30. (Currently Amended) The device according to claim 5, wherein ~~said plurality of first group III nitride compound semiconductor layers comprises a plurality of stacks of said first group III nitride compound semiconductor layers,~~ each of said stacks being individually and separately formed on said first environment division.

31. (Previously presented) The device according to claim 5, wherein a thickness of said plurality of first group III nitride compound semiconductor layers is less than a thickness of said separating layer.

32. (Previously presented) The structure according to claim 9, wherein a bottom of said plurality of openings is defined by said surface of said silicon substrate.